



# H77H2-M4

Rev : A

ECS CONFIDENTIAL

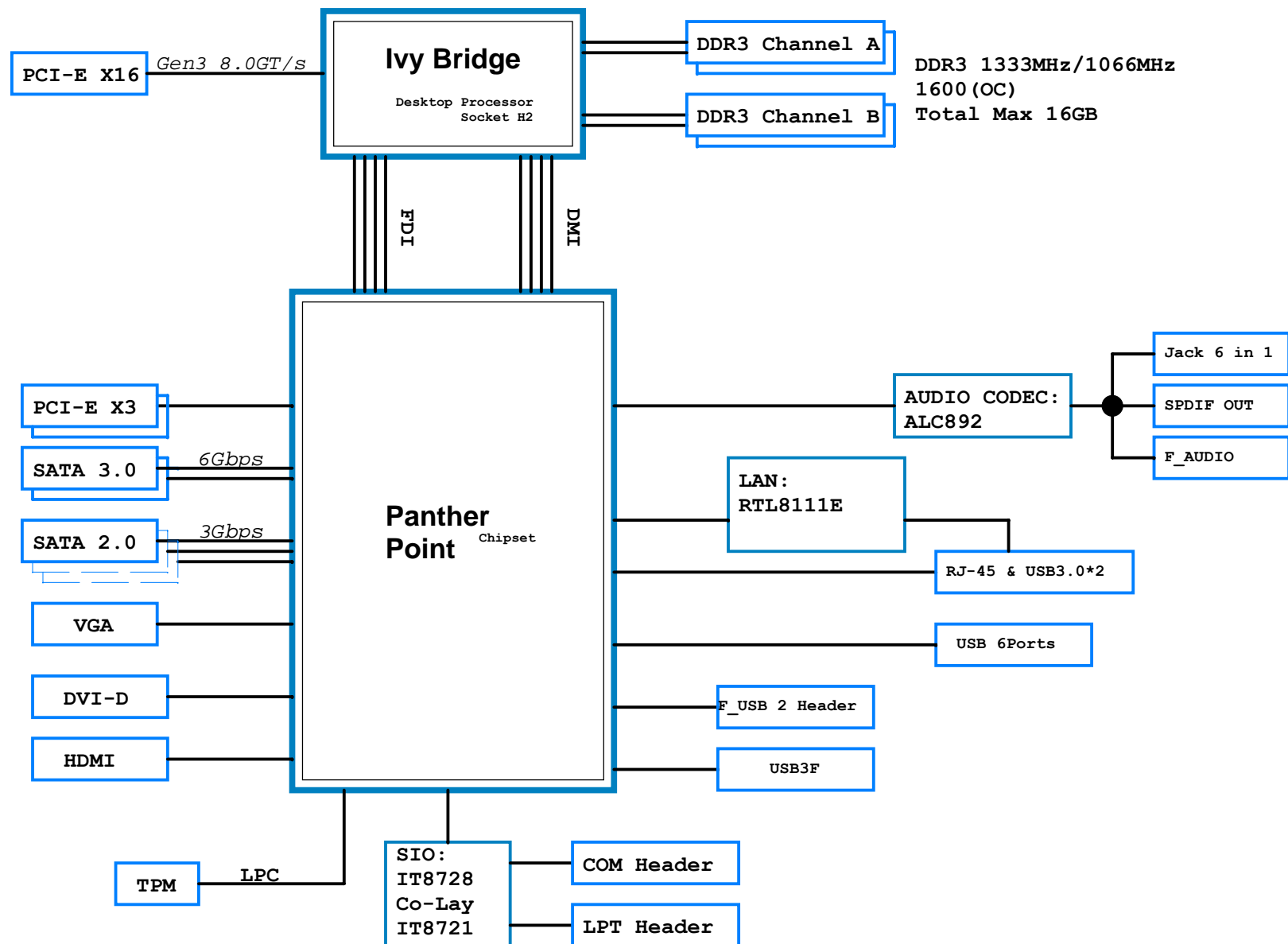
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REVISION HISTORY:

Rev	Date	Notes
VA		Initial version
VA	2011 09 01	page 31 Del LPC DEBUGE HEADER ADD TPM
VA	2011 09 08	page 30 SYS/PWR_FAN 3PIIN&4PIN CO_LAY
VA	2011 09 08	page 24 ADD DP CONNECT
VA	2011 09 08	page 20 ADD PCH DP CONNECT
VA	2011 09 13	page 25 Change USB Rear/Front
V1.0		
V1.0	2011 10 25	page 24 Change hdmi tx0 連線
V1.0	2011 11 28	page 30 Change MC113/MC125/MC126/MC111 TO 10U-16V-08
V1.0	2011 11 28	page 11 Change ER47 TO 75K OHM
V1.0	2011 11 29	page 25 Del CMF9/14/15
V1.0	2011 11 29	page 25 Remove CN2,3,4,5,6,7

- NOTE:
- 1. Model Code: EG7;
  - 2. Modified from H77H2-M4 V:A

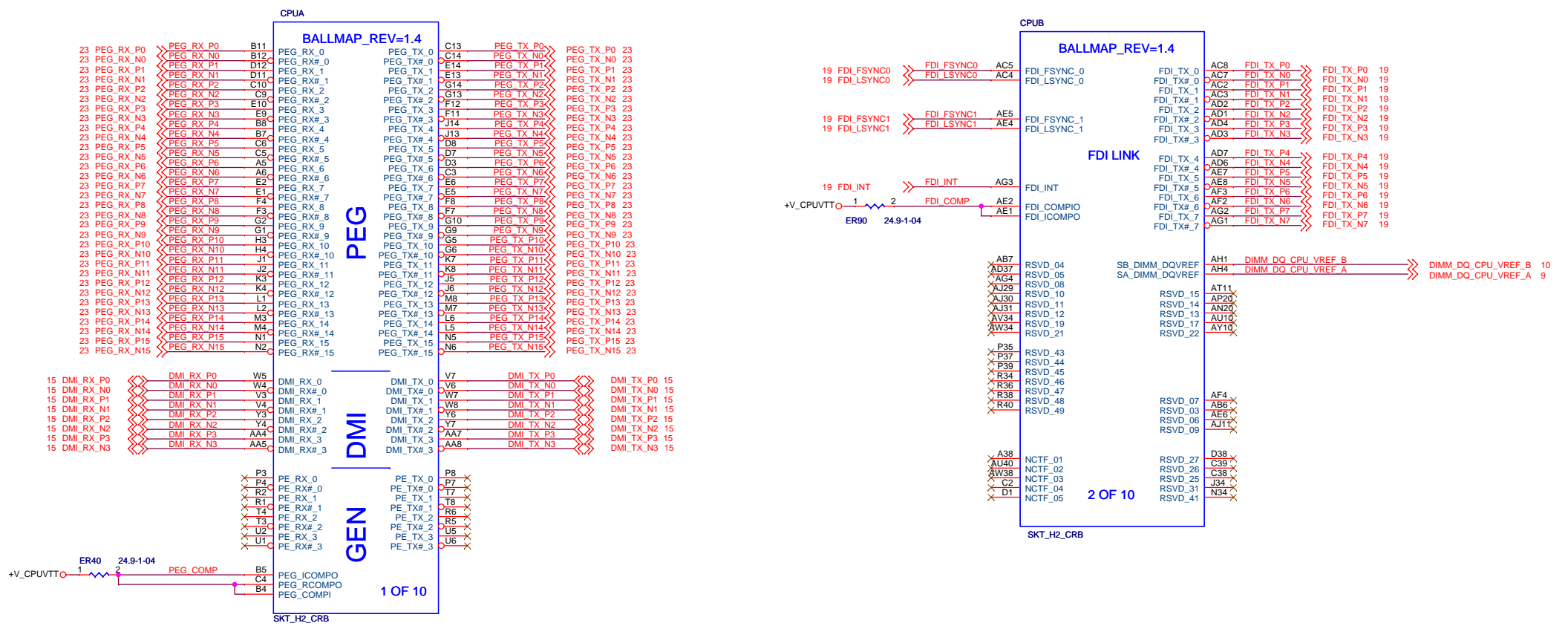


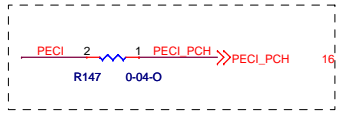
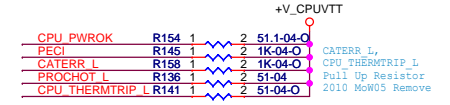
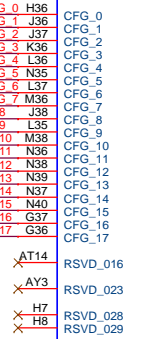
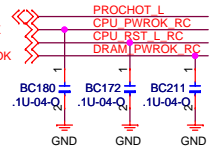
## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI

## SIO-GPIO function

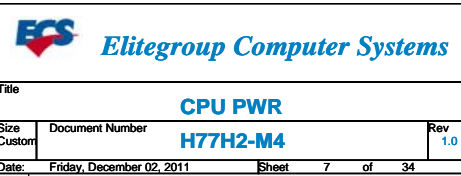
Pin Name	Power Well	Usage	Default Status
GP16		BEEP	
GP23		Power LED	
GP22		Power LED	
GP26		Over Voltage +V_1P05_PCH	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	





PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1



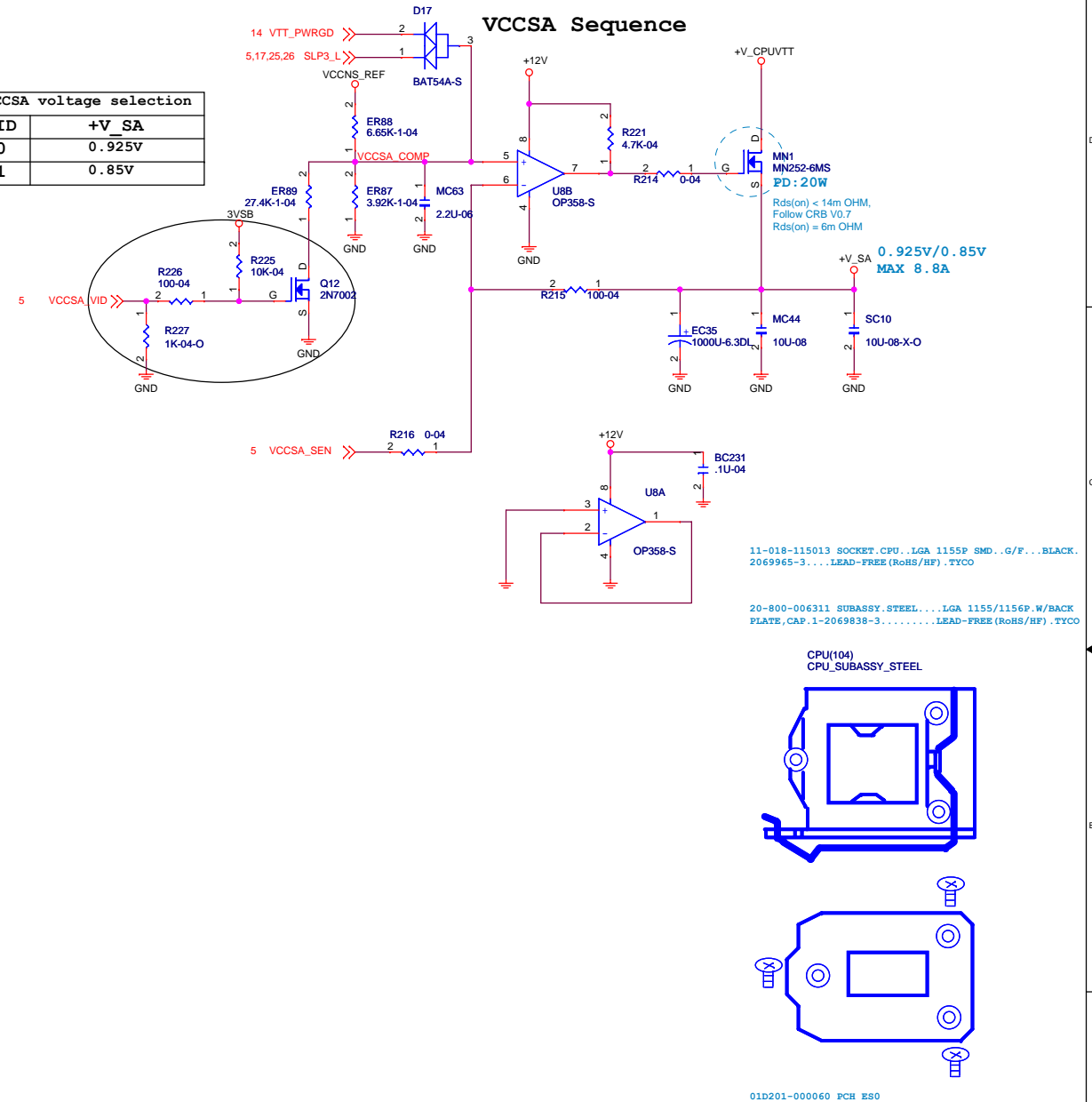




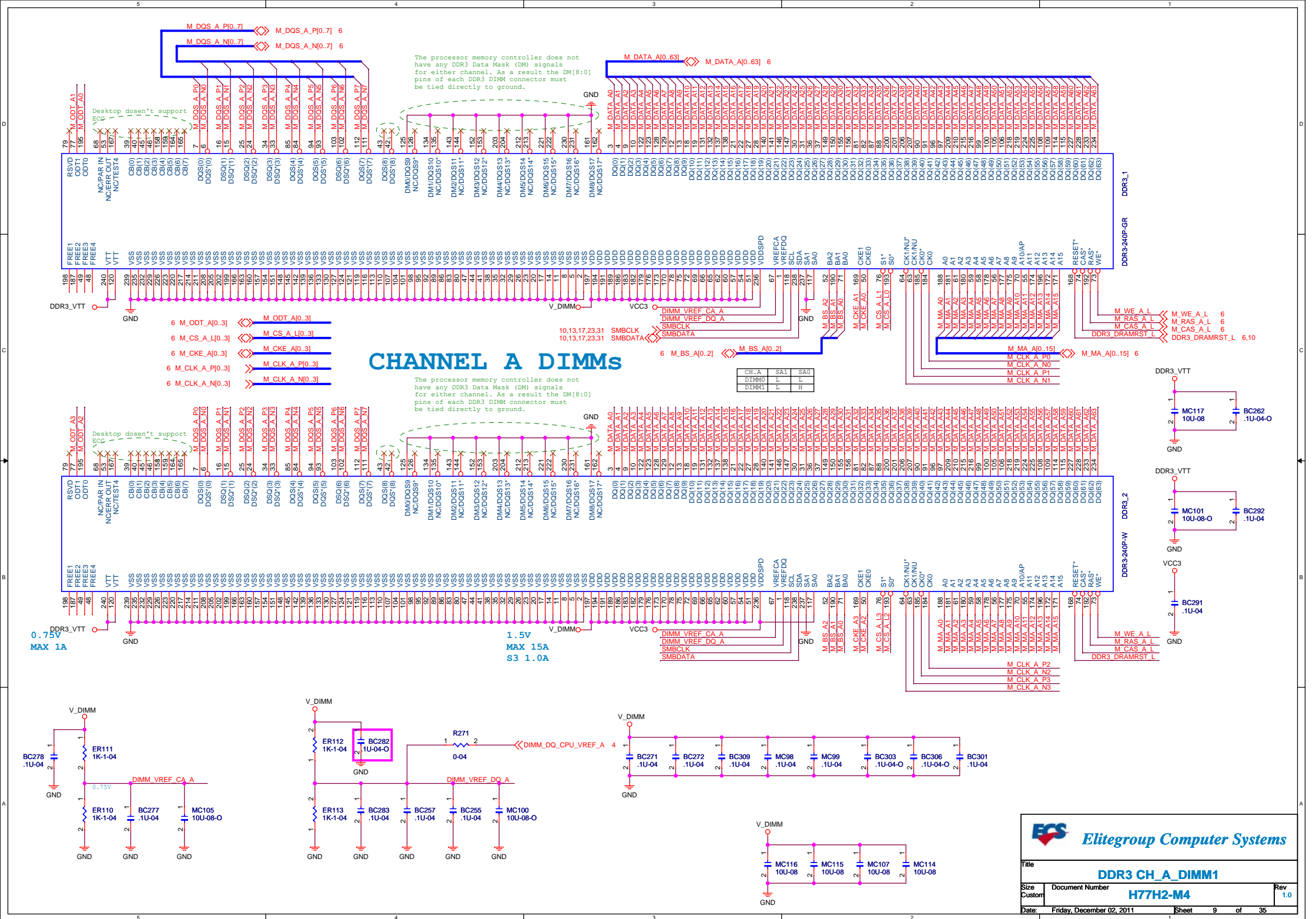
CPU1			CPU2		
BALLMAP_REV=1.4			BALLMAP_REV=1.4		
A17	VSS_001	AM27	AV11	VSS_181	G8
A23	VSS_002	AM3	AV14	VSS_182	H1
A26	VSS_003	AM30	AV17	VSS_183	H17
A29	VSS_004	AM36	AV3	VSS_184	H2
AA35	VSS_005	AM37	AV35	VSS_185	H20
AA33	VSS_006	AM38	AV38	VSS_186	H23
AA34	VSS_007	AM39	AV6	VSS_187	H26
AA35	VSS_008	AM4	AW10	VSS_188	H29
AA36	VSS_009	AM40	AW11	VSS_189	H33
AA37	VSS_010	AM5	AW14	VSS_190	H35
AA38	VSS_011	AN10	AW16	VSS_191	H37
AA6	VSS_012	AN11	AW36	VSS_192	H39
AB5	VSS_013	AN14	AW6	VSS_193	H5
AC1	VSS_014	AN17	AY11	VSS_194	H6
AC6	VSS_015	AN19	AY14	VSS_195	H9
AD33	VSS_016	AN22	AY18	VSS_196	J11
AD36	VSS_017	AN24	AY35	VSS_197	J17
AD38	VSS_018	AN30	AY4	VSS_198	J20
AD39	VSS_019	AN31	AY6	VSS_199	J23
AD40	VSS_020	AN32	AY8	VSS_200	J26
AD5	VSS_021	AN33	B10	VSS_201	J29
AD8	VSS_022	AN34	B11	VSS_202	J32
AE3	VSS_023	AN35	B14	VSS_203	K1
AE33	VSS_024	AN36	B17	VSS_204	K12
AE36	VSS_025	AN5	B23	VSS_205	K13
AF1	VSS_026	AN6	B26	VSS_206	K14
AF34	VSS_027	AN7	B29	VSS_207	K17
AF36	VSS_028	AN8	B35	VSS_208	K2
AF37	VSS_029	AN9	B38	VSS_209	K20
AF40	VSS_030	AP1	B6	VSS_210	K23
AF5	VSS_031	AP11	C11	VSS_211	K26
AF6	VSS_032	AP14	C12	VSS_212	K29
AG36	VSS_033	AP17	C17	VSS_213	K33
AH2	VSS_034	AP22	C20	VSS_214	K35
AH3	VSS_035	AP25	C23	VSS_215	K37
AH33	VSS_036	AP27	C26	VSS_216	K39
AH36	VSS_037	AP30	C29	VSS_217	K5
AH37	VSS_038	AP36	C32	VSS_218	K6
AH38	VSS_039	AP37	C35	VSS_219	L10
AH39	VSS_040	AP4	C7	VSS_220	L17
AH40	VSS_041	AP40	C8	VSS_221	L20
AH5	VSS_042	AP5	D17	VSS_222	L23
AH8	VSS_043	AR11	D2	VSS_223	L26
AJ12	VSS_044	AR14	D20	VSS_224	L29
AJ15	VSS_045	AR17	D23	VSS_225	L8
AJ18	VSS_046	AR18	D26	VSS_226	M1
AJ21	VSS_047	AR19	D29	VSS_227	M17
AJ25	VSS_048	AR27	D32	VSS_228	M2
AJ27	VSS_049	AR30	D37	VSS_229	M20
AJ36	VSS_050	AR36	D39	VSS_230	M23
AJ5	VSS_051	AR5	D4	VSS_231	M26
AK1	VSS_052	AT1	D5	VSS_232	M29
AK10	VSS_053	AT10	D9	VSS_233	M33
AK13	VSS_054	AT12	E11	VSS_234	M35
AK14	VSS_055	AT13	E17	VSS_235	M37
AK16	VSS_056	AT15	E20	VSS_236	M39
AK22	VSS_057	AT16	E23	VSS_237	M5
AK28	VSS_058	AT17	E26	VSS_238	M6
AK31	VSS_059	AT2	E29	VSS_239	M9
AK32	VSS_060	AT25	E32	VSS_240	N8
AK33	VSS_061	AT27	E36	VSS_241	P1
AK34	VSS_062	AT28	E7	VSS_242	P2
AK35	VSS_063	AT29	E8	VSS_243	P36
AK36	VSS_064	AT3	F1	VSS_244	P38
AK37	VSS_065	AT30	F10	VSS_245	P40
AK4	VSS_066	AT31	F13	VSS_246	P5
AK40	VSS_067	AT32	F14	VSS_247	P6
AK5	VSS_068	AT33	F17	VSS_248	P36
AK6	VSS_069	AT34	F2	VSS_249	P38
AK7	VSS_070	AT35	F20	VSS_250	R37
AK8	VSS_071	AT36	F23	VSS_251	R39
AK9	VSS_072	AT38	F29	VSS_252	R8
AL11	VSS_073	AT39	F35	VSS_253	T1
AL14	VSS_074	AT4	F37	VSS_254	T5
AL17	VSS_075	AT5	F5	VSS_255	T6
AL19	VSS_076	AT6	F6	VSS_256	T8
AL24	VSS_077	AT7	F9	VSS_257	V1
AL27	VSS_078	AT8	G11	VSS_258	V2
AL30	VSS_079	AT9	G12	VSS_259	V33
AL36	VSS_080	AT15	G20	VSS_260	V34
AL5	VSS_081	AT16	G23	VSS_261	V35
AM1	VSS_082	AT17	G26	VSS_262	V36
AM11	VSS_083	AT18	G29	VSS_263	V37
AM14	VSS_084	AT19	G34	VSS_264	V38
AM17	VSS_085	AT20	G7	VSS_265	V39
AM2	VSS_086	AT21	AY37	VSS_266	V40
AM21	VSS_087	AT22	B3	VSS_267	V5
AM23	VSS_088	AT23	VSS_NCTF_03	VSS_268	W6
AM25	VSS_089	AT24	VSS_NCTF_04	VSS_269	Y5
AM25	VSS_090	AT25		VSS_270	Y8

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

\*



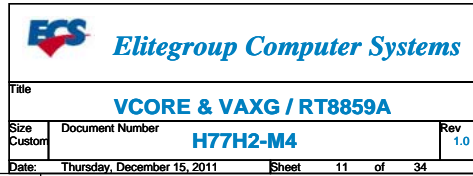






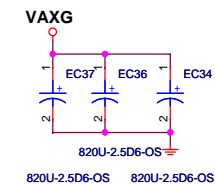
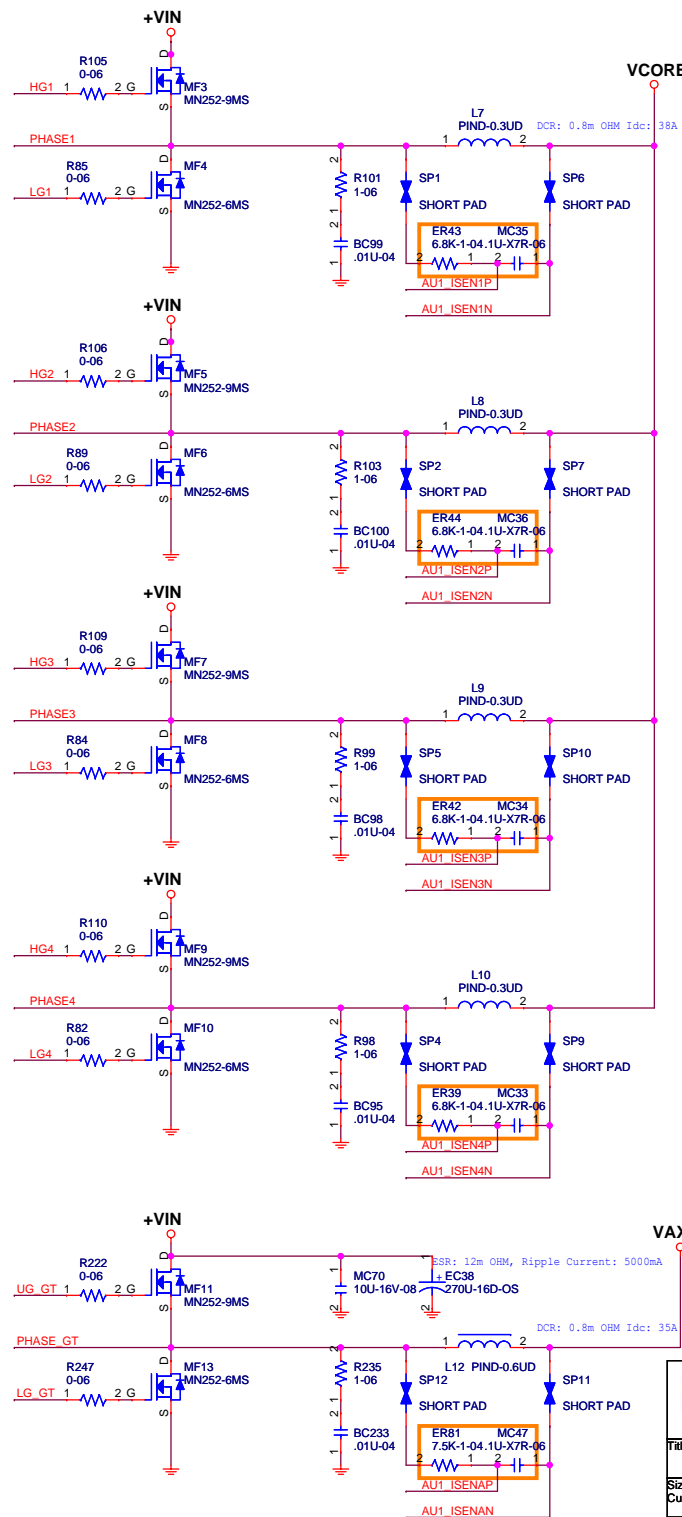
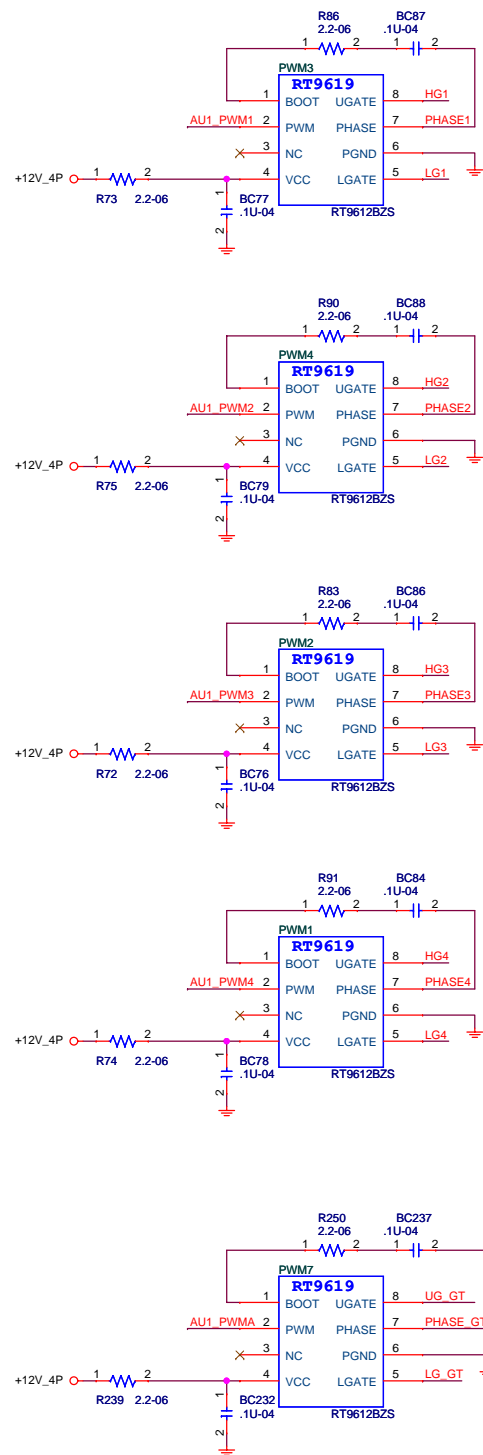
## External Connection

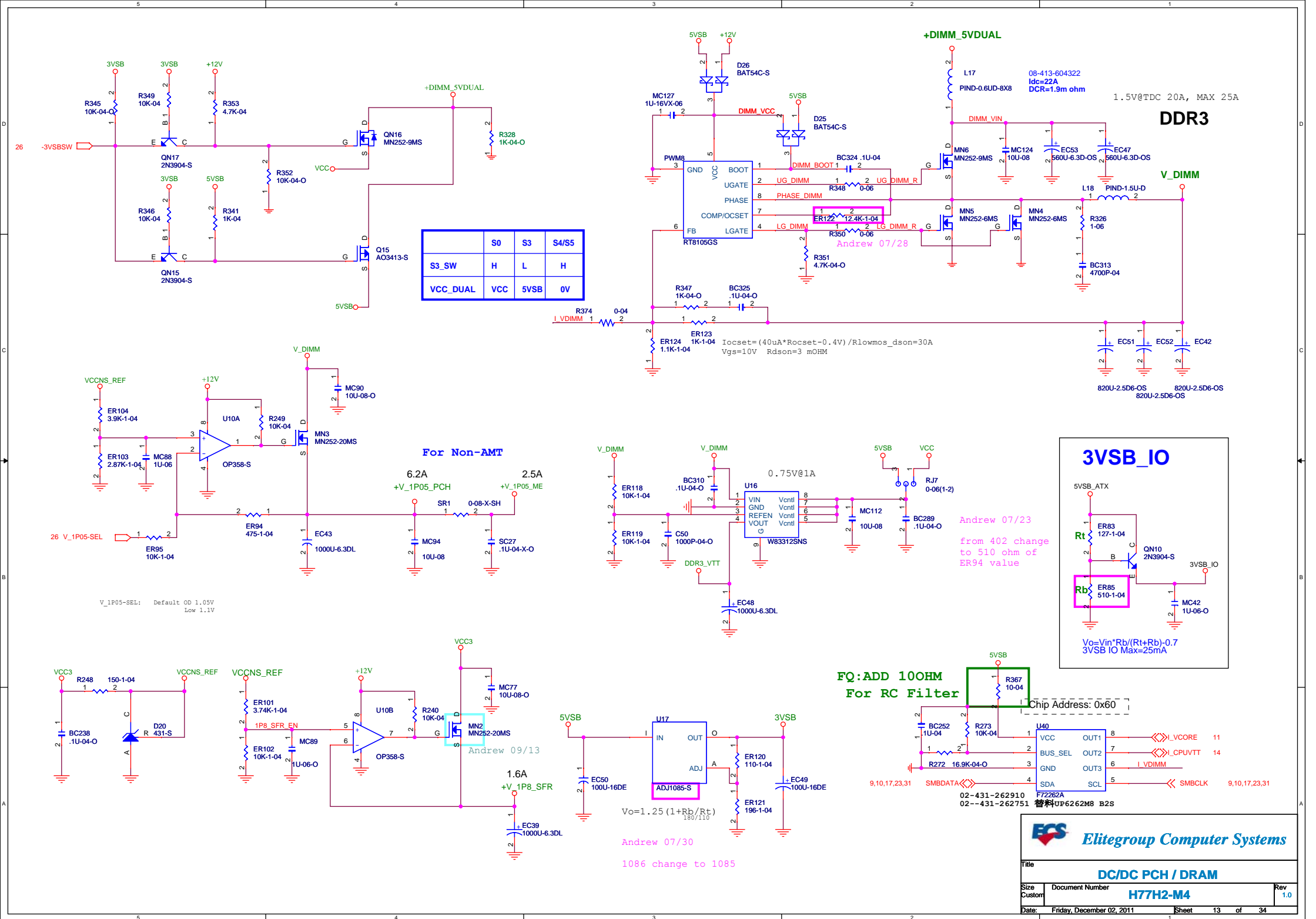
Pin	Signal	External Connection
1	VCC	VCC
2	+V_CPUVTT	+AVTT
3	+12V_4P	+12V_4P
4	VCC3	+VCC3
5	+VIN	+VIN
6	5VSB	+VSB
7	VR_EN	VR_EN
8	VR_SVID_ALERT_L	ALERT
9	VR_SVID_DATAOUT	VDDIO
10	VR_SVID_CK	VCLK
11	VR_HOT_L	AUT_VRHOT
12	AUT_PWM1[1..4]	AUT_PWM1[1..4]
13	AU1_ISEN1P	AU1_ISEN1P
14	AU1_ISEN1N	AU1_ISEN1N
15	AU1_ISEN2P	AU1_ISEN2P
16	AU1_ISEN2N	AU1_ISEN2N
17	AU1_ISEN3P	AU1_ISEN3P
18	AU1_ISEN3N	AU1_ISEN3N
19	AU1_ISEN4P	AU1_ISEN4P
20	AU1_ISEN4N	AU1_ISEN4N
21	VCC_SEN	VCC_SEN
22	VSS_SEN	VSS_SEN
23	VR_READY	VR_READY
24	AU1_PWMMA	AU1_PWMMA
25	AU1_ISENAP	AU1_ISENAP
26	AU1_ISENAN	AU1_ISENAN
27	VCCAXG_SEN	VCCAXG_SEN
28	VSSAXG_SEN	VSSAXG_SEN
29	AXG_GP1	AXG_GP1
30	AXG_GP2	AXG_GP2
31	I_VCORE	I_VCORE
32	H_SKTOCC_L	H_SKTOCC_N



A diagram showing the pin-to-pin connections for the module. It consists of two vertical columns of pins, each with a label to its left. The labels are: VCC, VCORE, +V\_CPUVTT, +12V\_4P, VCC3, and +VIN. Each label is connected to a pin on the left, and a corresponding pin on the right is connected to the same label. The connections are as follows:

Left Pin Label	Right Pin Label
VCC	VCC
VCORE	VCORE
+V_CPUVTT	AVTT
+12V_4P	+12V_4P
VCC3	VCC3
+VIN	+VIN

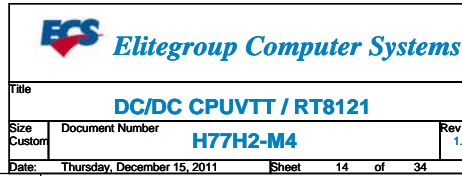


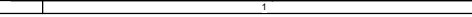


Pin	Signal
VCC	+VCC
+12V_4P	+12V_4P
3VSB	3VSB
5VSB	5VSB
+V_1P05_PCH	+V_1P05_PCH
+V_CPUVTT	+V_CPUVTT
VTT_SEL	VTT_SEL
VTT_PWGRD	VTT_PWGRD
VCCIO_SEN	VCCIO_SEN
VSSIO_SEN	VSSIO_SEN
I_CPUVTT	I_CPUVTT

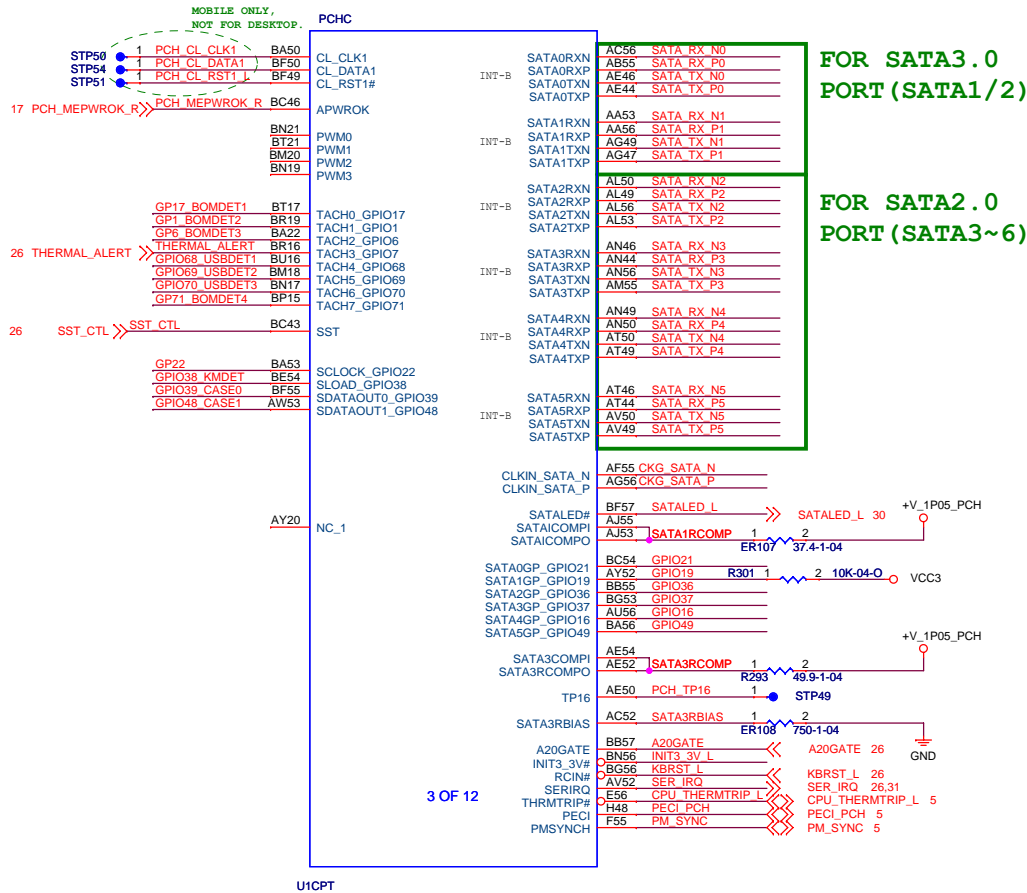
Andrew 09/09

Follow RichT





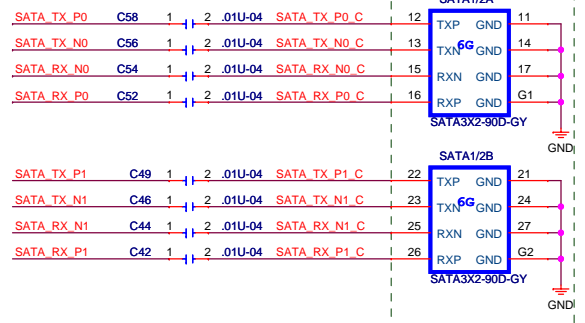




FOR SATA3.0  
PORT (SATA1/2)

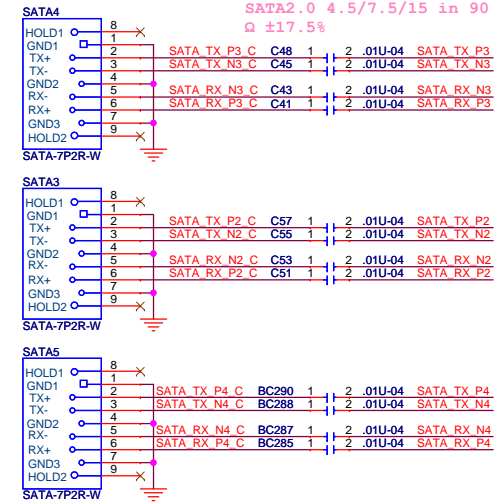
FOR SATA2.0  
PORT (SATA3~6)

## SATA3.0



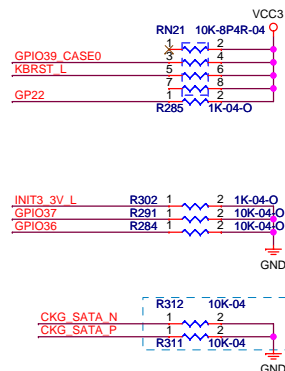
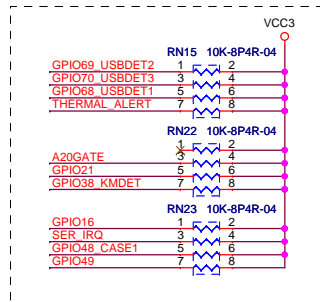
## SATA2.0

Layout Note:  
SATA3.0 4.5/7.5/20 in 85  
Q ±17.5%  
SATA2.0 4.5/7.5/15 in 90  
Q ±17.5%



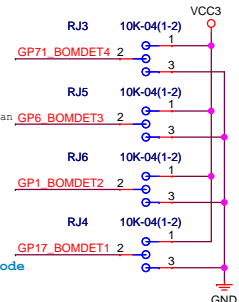
	SYS/PWR_FAN 3PIN	SYS/PWR_FAN 4PIN
SP17_BOMDET1	high	low
HDMI+DP		HDMI
SP1_BOMDET2	high	low

Default GPI set to Pull Up:



1 為GALAN, 0 為100Mlan

Stuff for  
Integrated Clock Mode

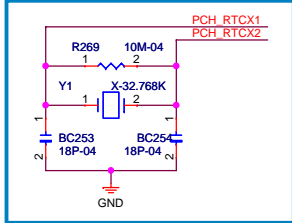
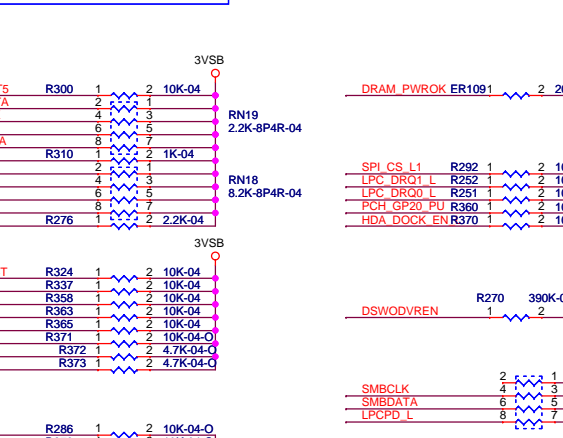
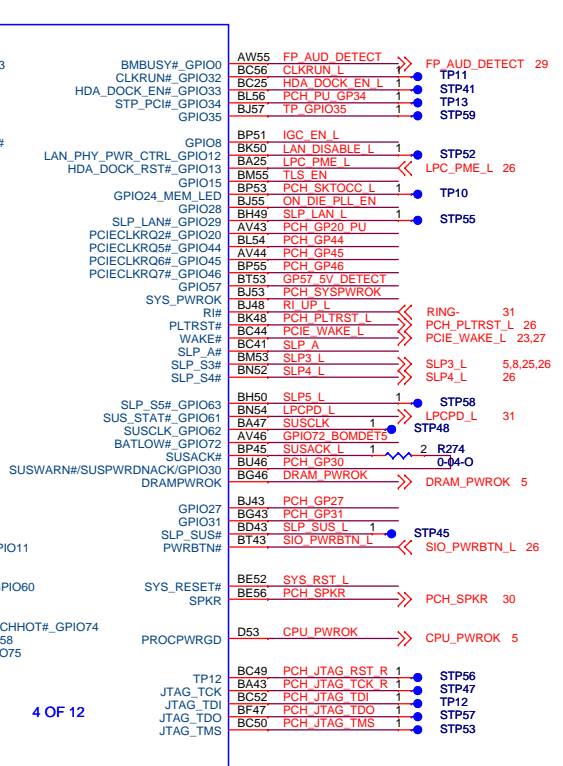
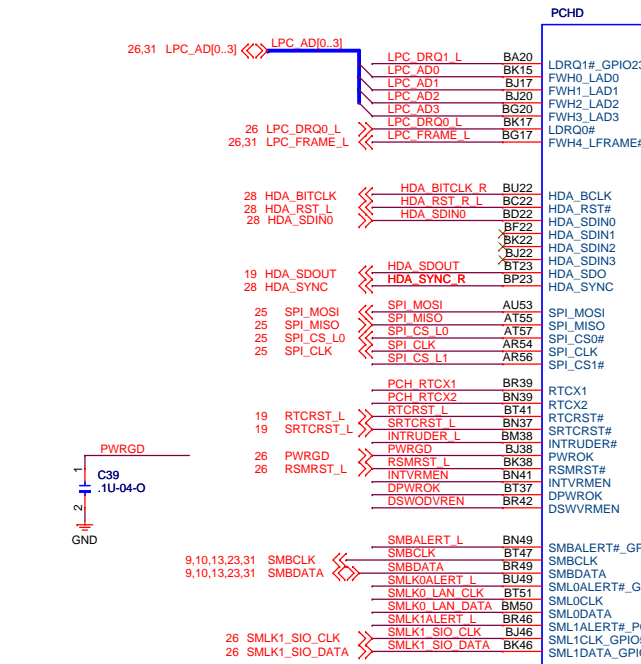


	SYS/PWR_FAN 3PIN	SYS/PWR_FAN 4PIN
SP17_BOMDET1	high	low
HDMI+DP		HDMI
SP1_BOMDET2	high	low

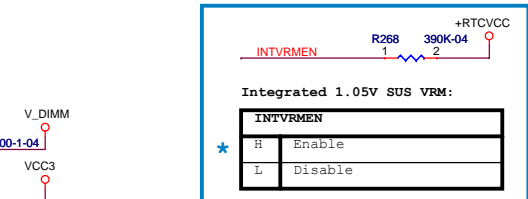
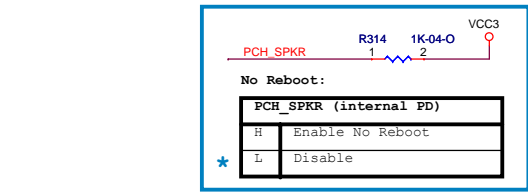
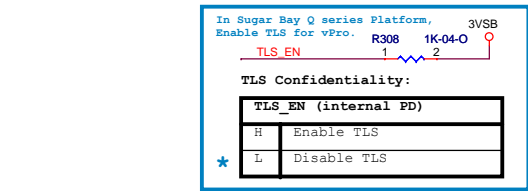
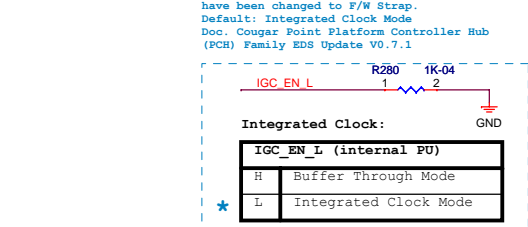
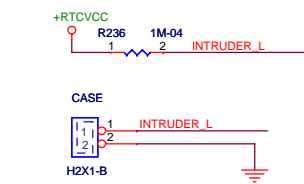
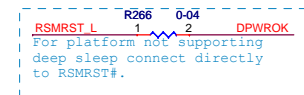


Elitegroup Computer Systems

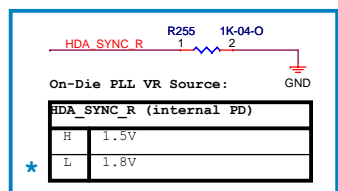
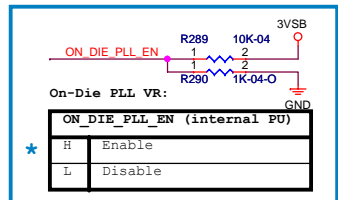
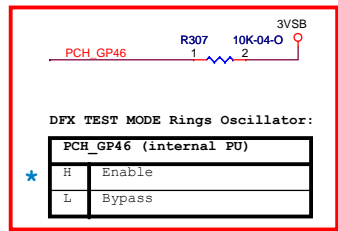
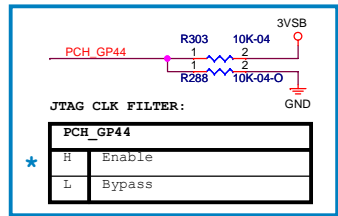
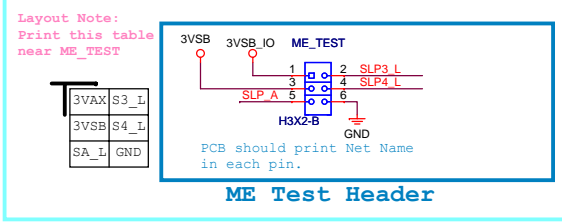
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Size	Document Number
Custom	H77H2-M4
Date	Friday, December 02, 2011
Sheet	16 of 34
Rev	1.0



When Deep Sleep not implemented:  
1. PCH\_GP30, PCH\_GP27 need to be Pull Up.  
2. VCCDSW3\_3 should be connected to +3VSB.  
3. SLP\_SUS\_L, SUSACK\_L left unconnected.  
4. SUSWARN#\_L may be used as GPIO30. (Reference to 1.)

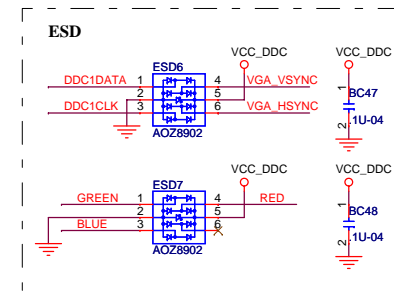


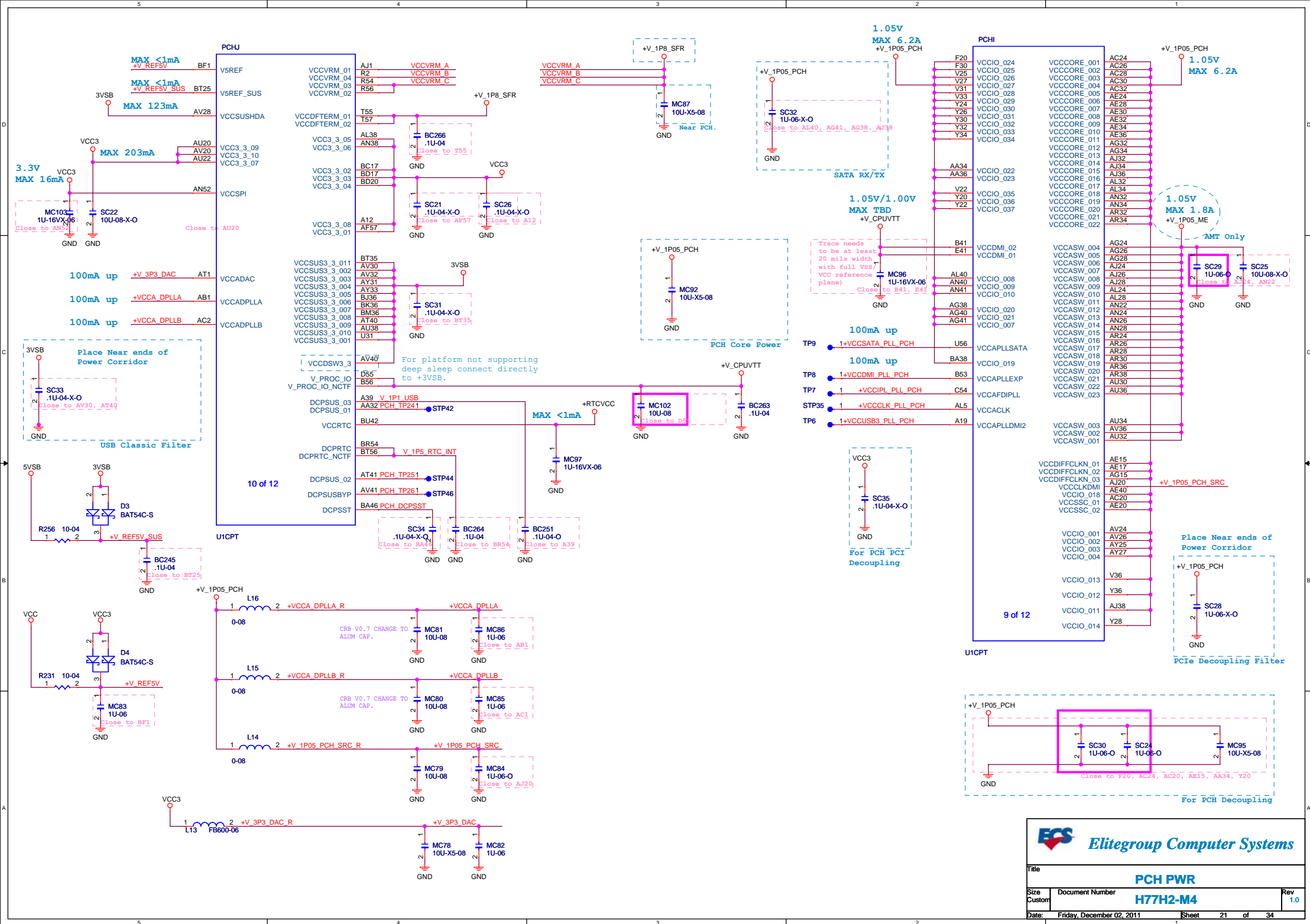
Andrew 09/09 For PV verify







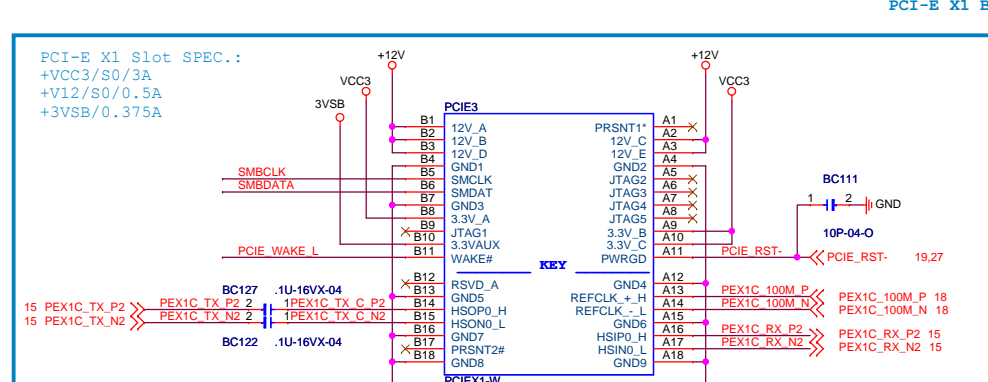
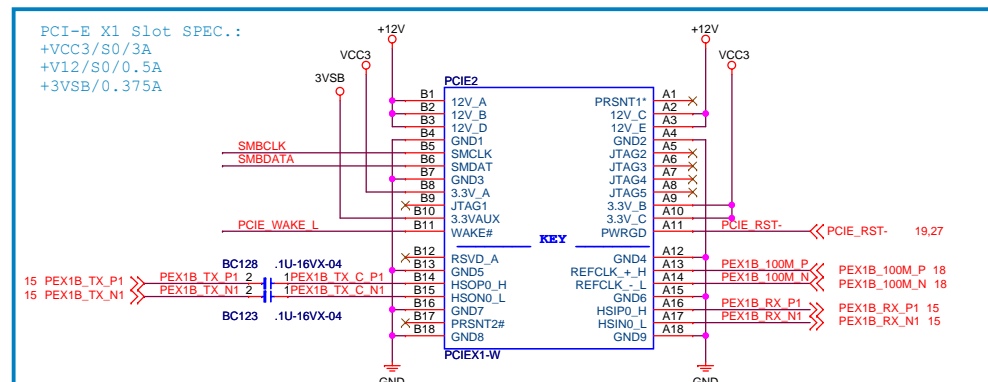
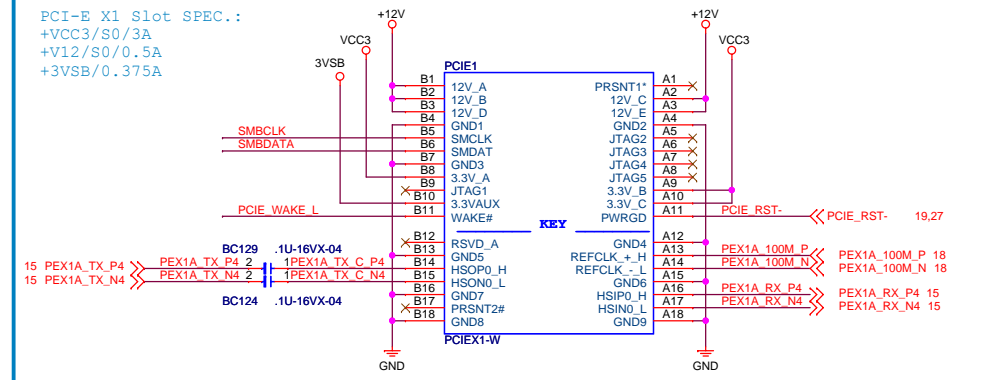
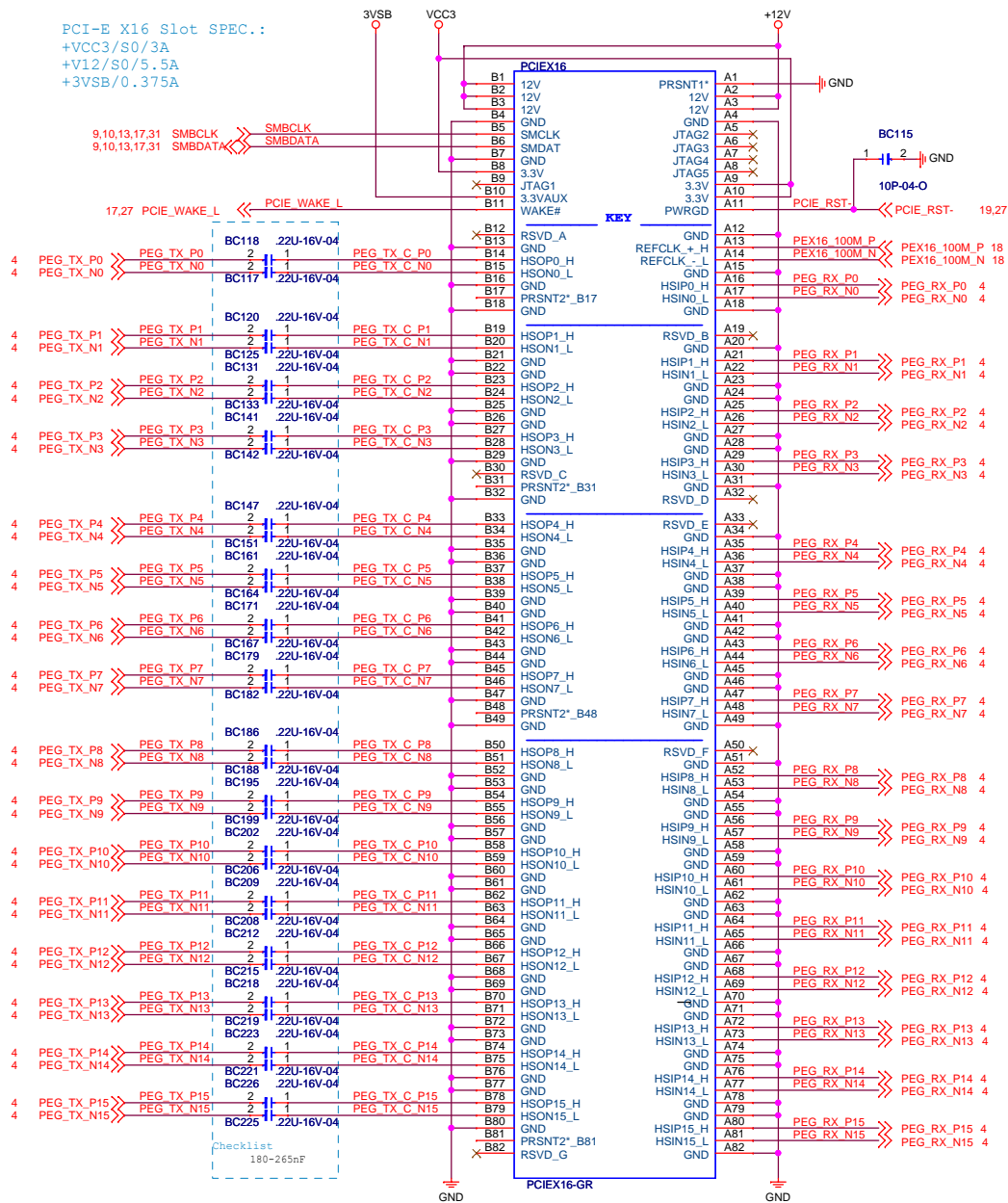




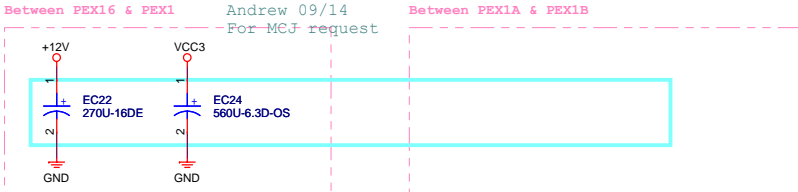
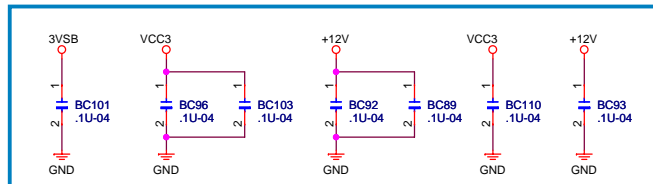




PCI-E X16 Slot SPEC.:  
+VCC3/S0/3A  
+V12/S0/5.5A  
+3VSB/0.375A



PCI-E A Decoupling Cap.



**Elitegroup Computer Systems**

Title: Slot PCI-EX16 / PCI-EX1

Size: Document Number H77H2-M4

Customer: Rev 1.0

Date: Friday, December 02, 2011 Sheet 23 of 34

20 DDPD\_HDP\_F << DDPD\_HDP\_F

0 DDPD\_CTRLCLK << DDPD\_CTRLCLK

DDPD\_CTRLDATA << DDPD\_CTRLDATA

20 DDPD\_TX0 << DDPD\_TX0

20 DDPD\_TX0 << DDPD\_TX0-

20 DDPD\_TX1 << DDPD\_TX1

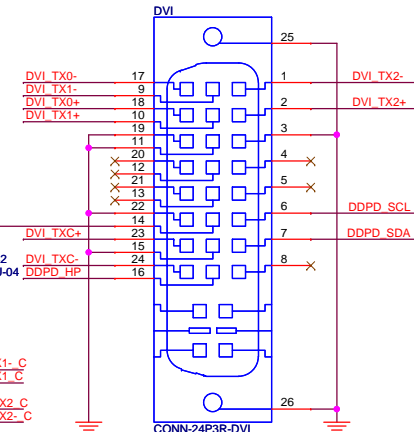
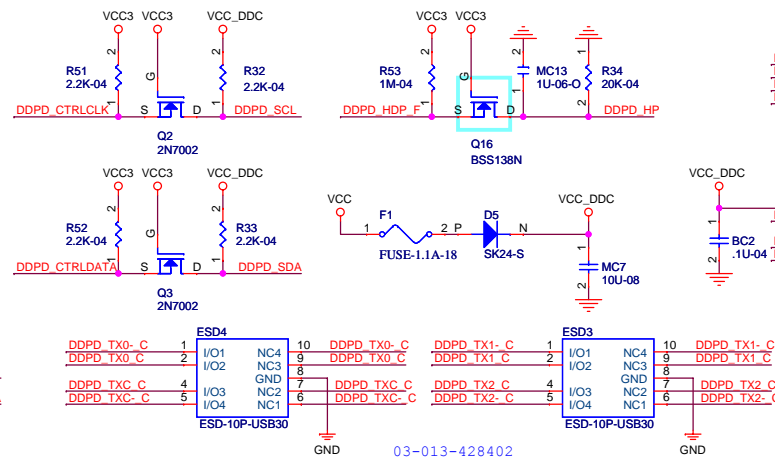
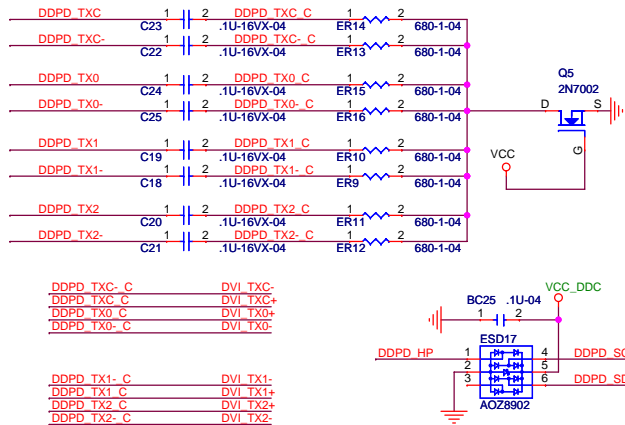
20 DDPD\_TX1 << DDPD\_TX1-

20 DDPD\_TX2 << DDPD\_TX2

20 DDPD\_TX2 << DDPD\_TX2-

20 DDPD\_TXC << DDPD\_TXC

20 DDPD\_TXC << DDPD\_TXC-

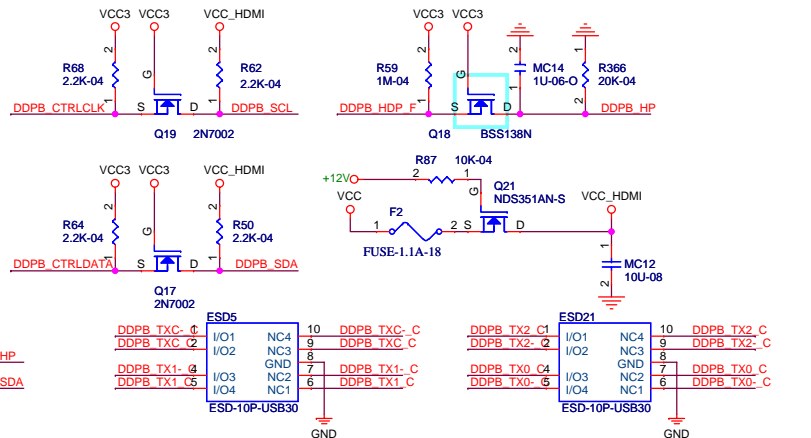
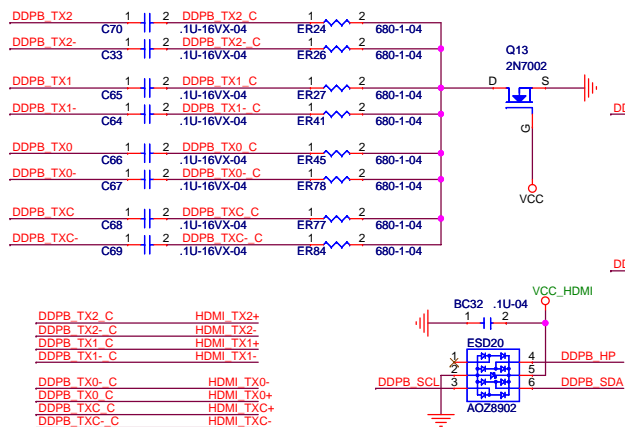


```

20 DDPB_HDP_F<< DDPB_HDP_F
20 DDPB_CTRLCLK >> DDPB_CTRLCLK
20 DDPB_CTRLDATA >> DDPB_CTRLDATA

20 DDPB_TX2< DDPB_TX2
20 DDPB_TX2< DDPB_TX2-
20 DDPB_TX1< DDPB_TX1
20 DDPB_TX1< DDPB_TX1-
20 DDPB_TX0< DDPB_TX0
20 DDPB_TX0< DDPB_TX0-
20 DDPB_TXC< DDPB_TXC
20 DDPB_TXC< DDPB_TXC-

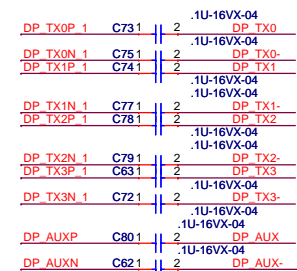
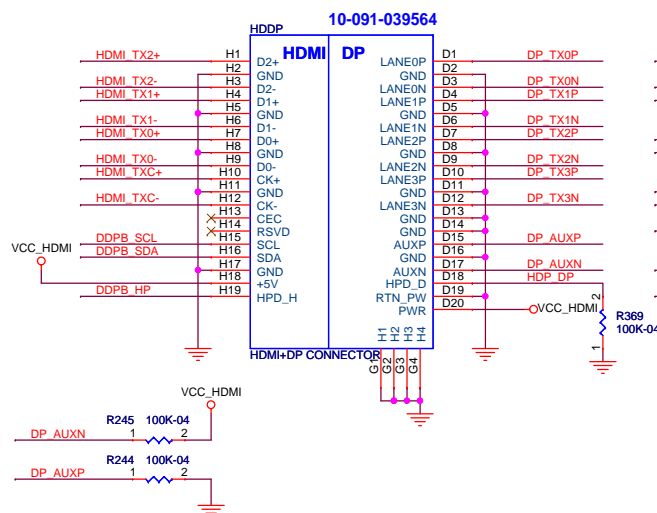
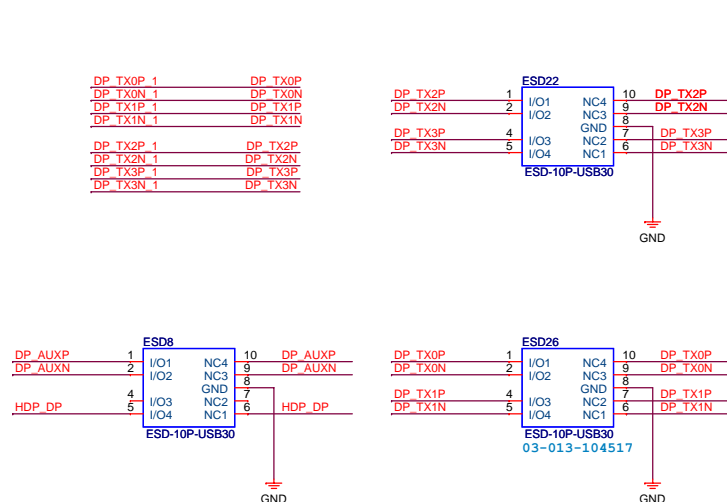
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HDMI CONNECT  
10-093-019690

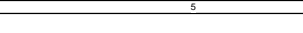
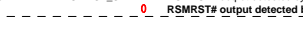
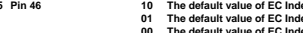
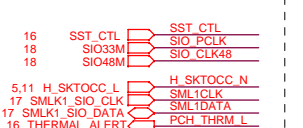
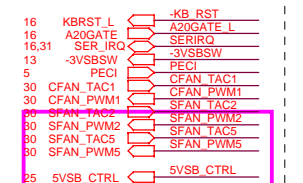
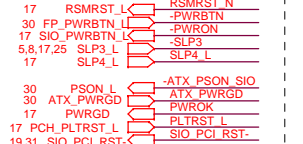
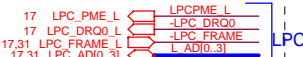
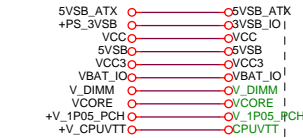
## RJ6 DET (HDIM+DP) &amp;HDMI

The diagram shows a set of connections between two components. On the left, there are labels: DP\_HDP, DP\_TX0, DP\_TX1, DP\_TX2, DP\_TX3, DP\_AUX, and DP\_AUX-. On the right, there are corresponding labels: DP\_HDP, DP\_TX0-, DP\_TX1-, DP\_TX2-, DP\_TX3-, DP\_AUX, and DP\_AUX-. Red arrows indicate the connections: a double arrow from DP\_HDP to DP\_HDP, single arrows from DP\_TX0 to DP\_TX0-, DP\_TX1 to DP\_TX1-, DP\_TX2 to DP\_TX2-, and DP\_TX3 to DP\_TX3-, and single arrows from DP\_AUX to DP\_AUX and DP\_AUX- to DP\_AUX-.





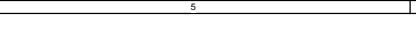
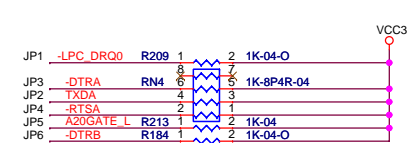
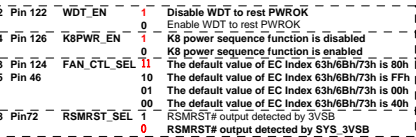
## External Connection



Andrew 07/23

From Pin 12 change to Pin 21

## HW STRAPPING

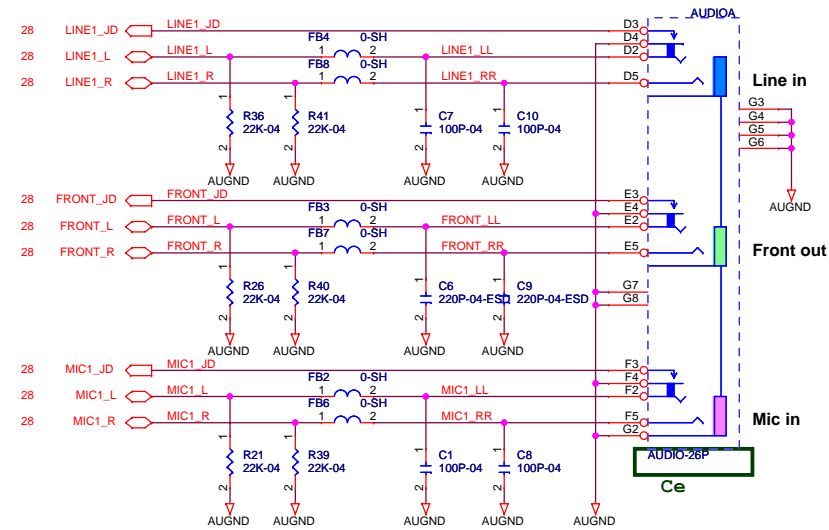




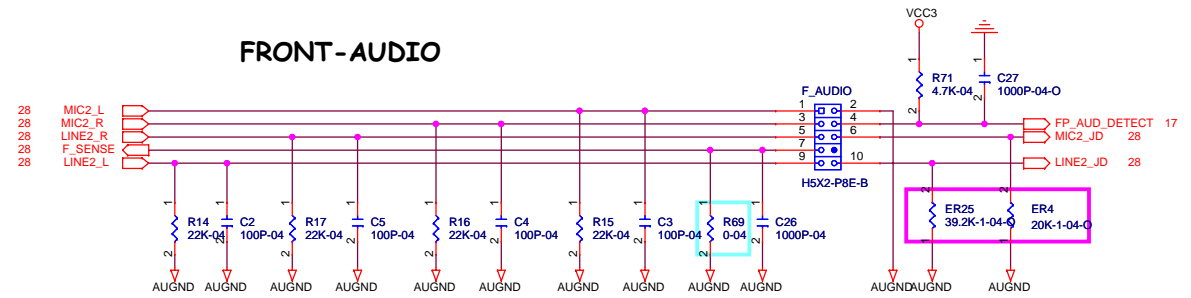




## REAR-AUDIO



## FRONT-AUDIO

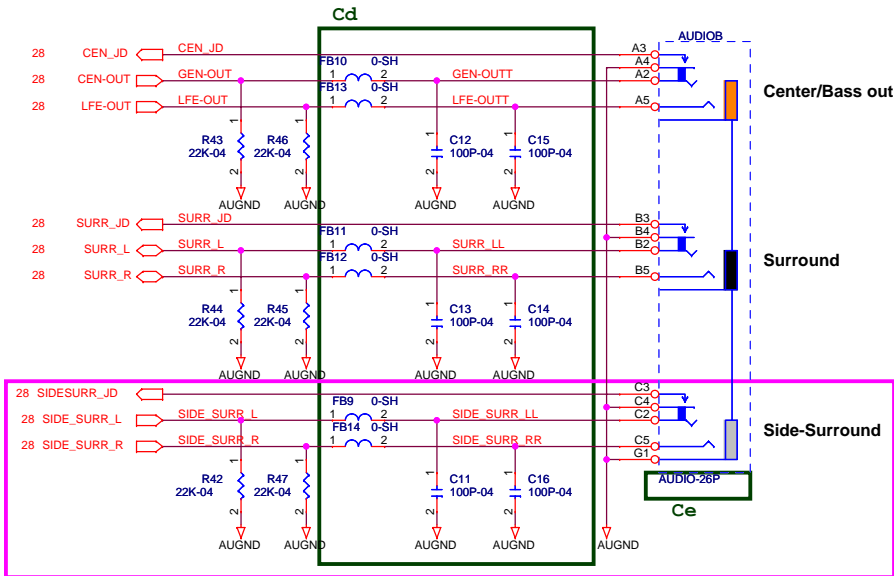
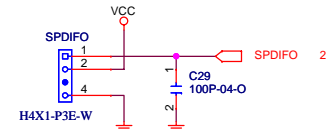


Andrew 09/01

Stuff R69

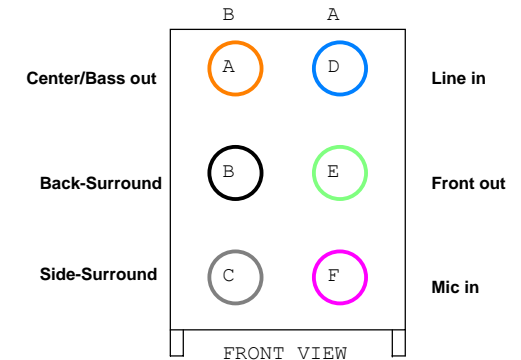
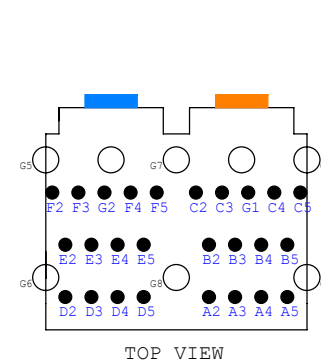
Line-out ( speak out) 的對地電容改成 for ESD的VPORT 電容 04-140-221005

## SPDIF-OUT



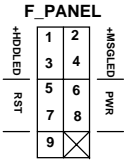
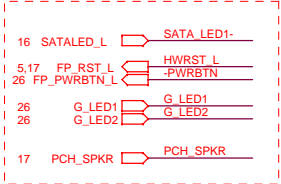
Andrew 07/28

Change to Side-Surround

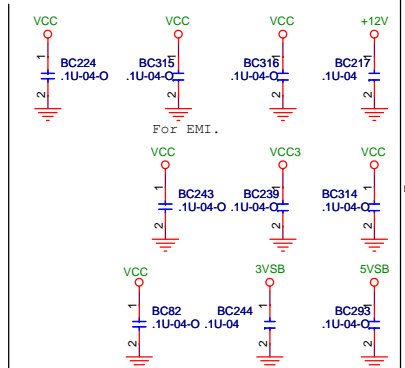
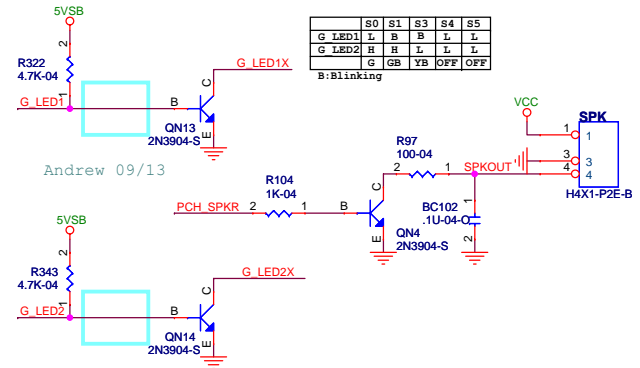
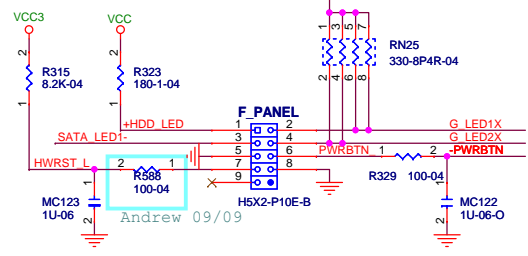




External Connection

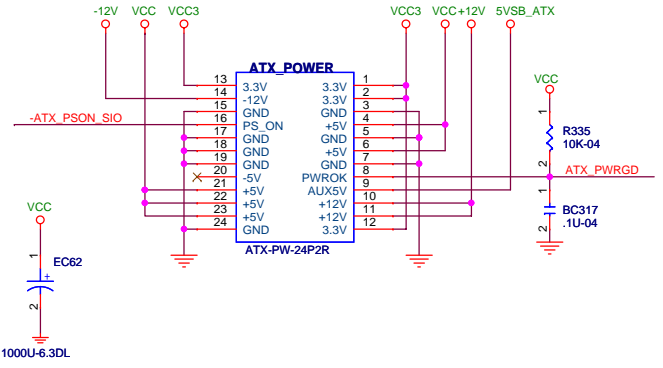
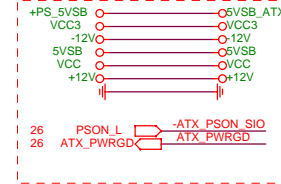


FRONT PANEL



POWER CONNECTOR

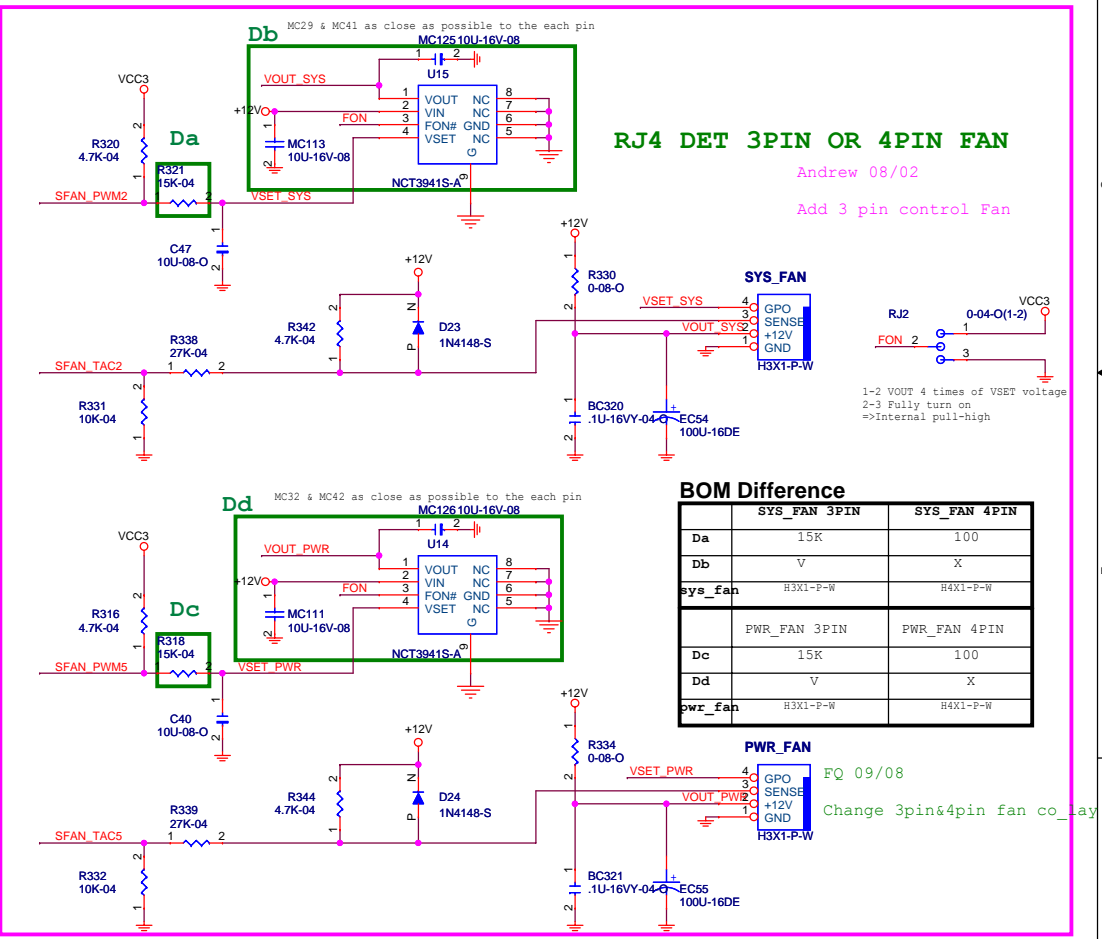
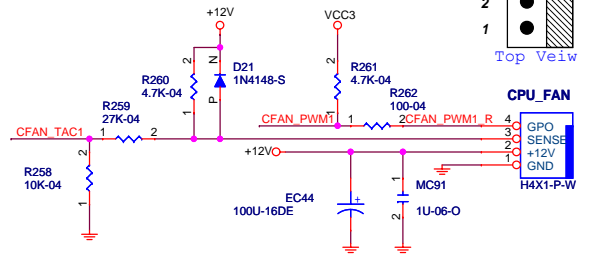
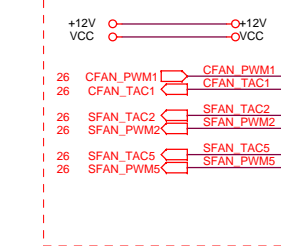
External Connection



FAN

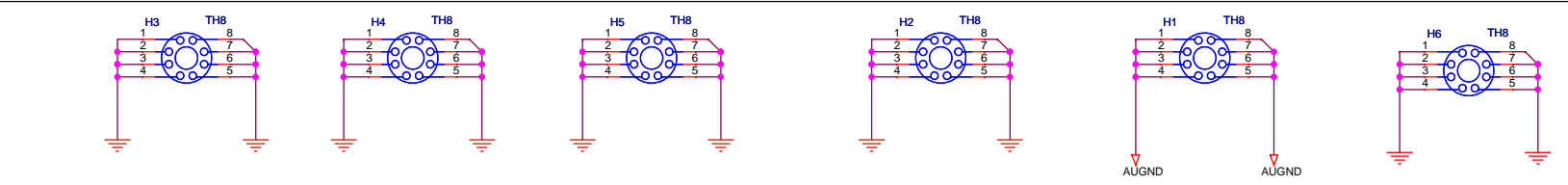
Kent 1016

External Connection



BOM Difference

	SYS_FAN 3PIN	SYS_FAN 4PIN
Da	15K	100
Db	V	X
sys_fan	H3X1-P-W	H4X1-P-W
	PWR_FAN 3PIN	PWR_FAN 4PIN
Dc	15K	100
Dd	V	X
pwr_fan	H3X1-P-W	H4X1-P-W



Title

F\_PANEL / FAN / PWR CONN

Size Custom

Document Number

H77H2-M4

Date

Thursday, December 15, 2011

Sheet

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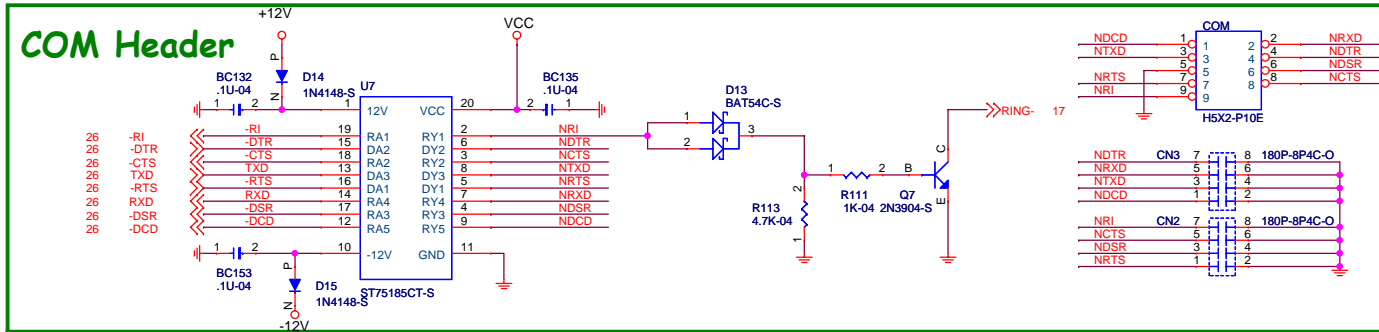
of

34

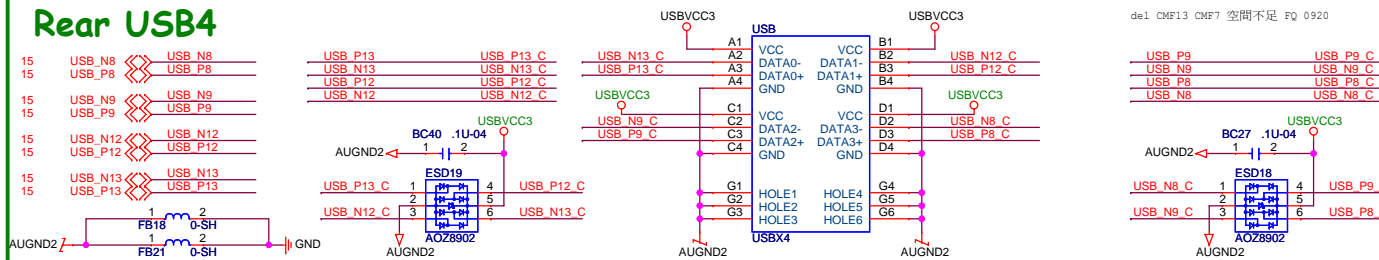
Rev

1.0

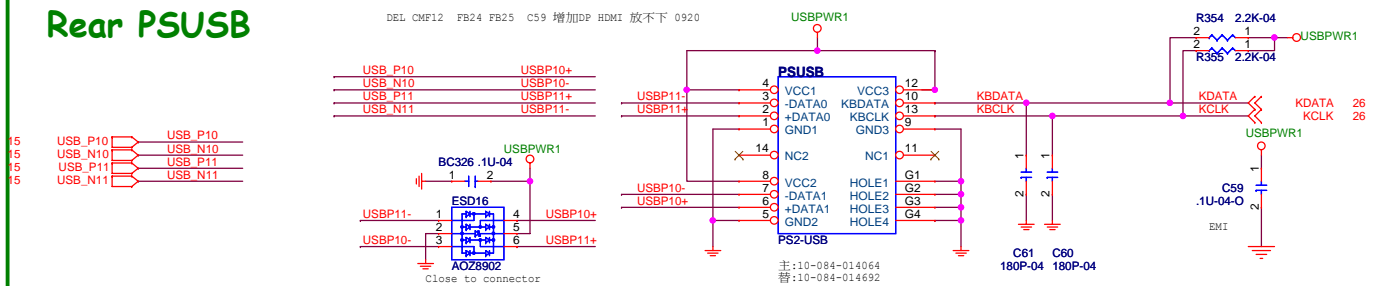
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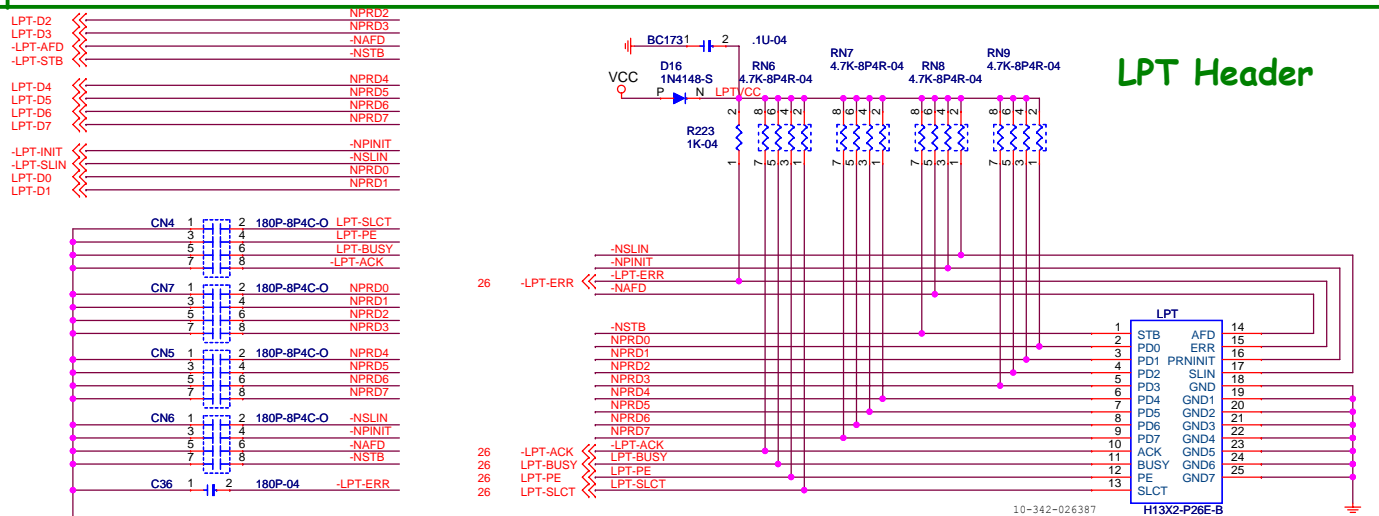
## Rear USB4



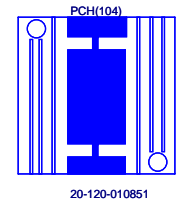
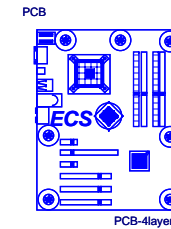
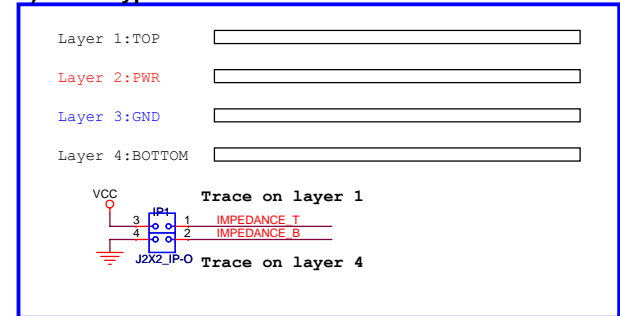
## Rear PSUSB



## LPT Header



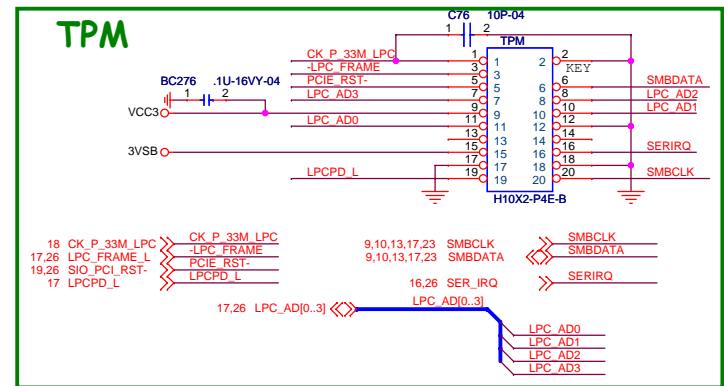
### 1)Circuit type 1



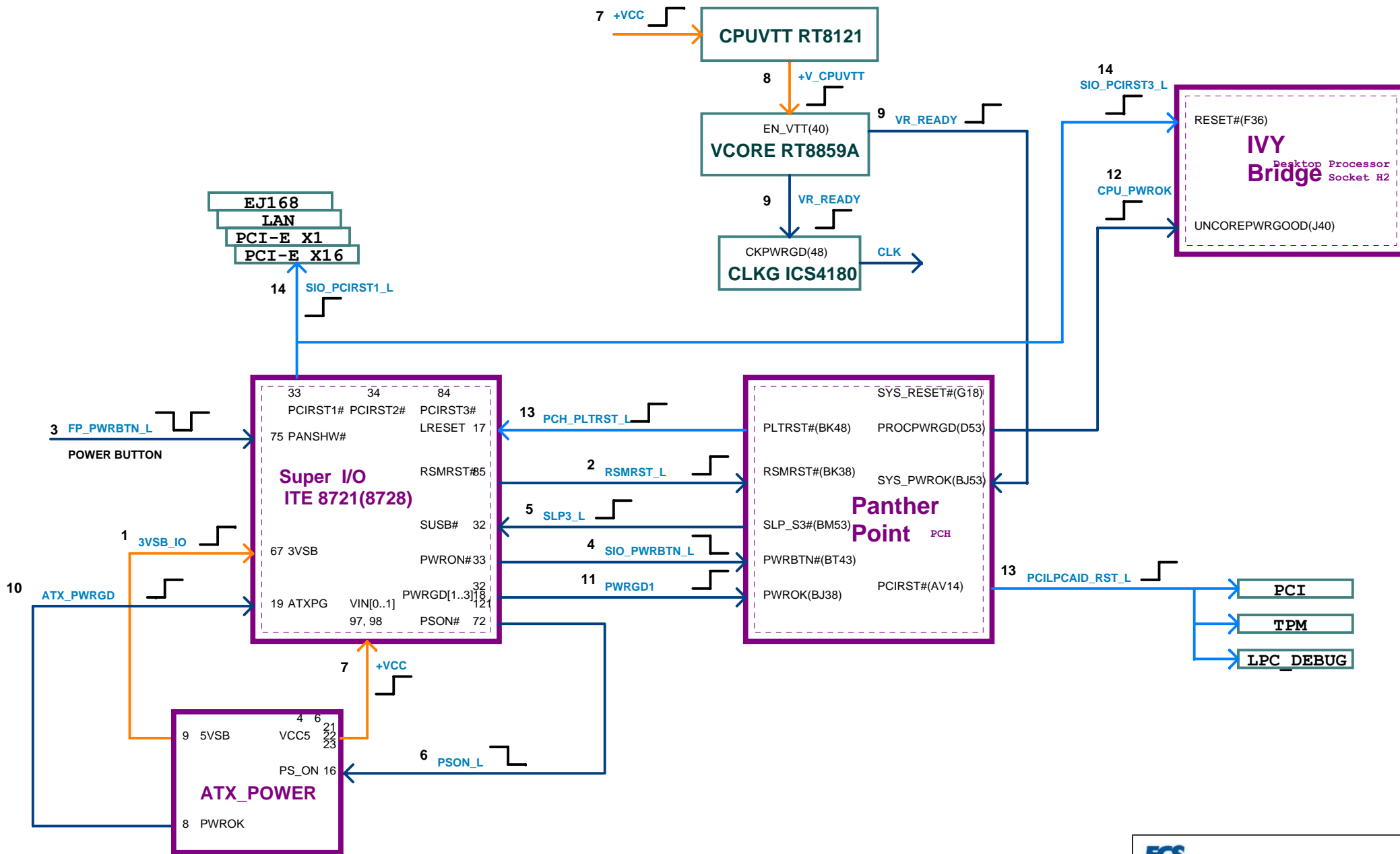
**PCB STACK:** L1:TOP  
L2:PWR  
L3:GND  
L4:BOTTOM



## TPM







**NOTE:**

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

